VISHWAKARMA GOVERNMENT ENGINEERING COLLEGE, CHANDKHEDA

Report on the Webinar on "Insights of ASIC Design Flow, Challenges and Future Trends in Semiconductor"

Name of Department	:	Electronics & Communication Engineering
Title of Webinar	:	Insights of ASIC Design Flow, Challenges and Future Trends in Semiconductor
Expert Name, Designation & Affiliation	:	Mr Nilesh Ranpura Delivery Manager, ASIC, e-Infochip, Ahmedabad
Date & Time	:	01/04/21, 3-5 pm
Venue	:	Microsoft Teams Platform (Online)
No of Participants	:	75
Event Coordinator	:	Prof J K Naik and Prof N P Patel

About the Webinar

The Electronics and Communication Engineering Department organized a webinar on "Insights of ASIC Design Flow, Challenges and Future Trends in Semiconductor" on April 1, 2021 from 3-5 pm to make the students aware of the current and future trends in VLSI domain.

Objectives of the Webinar

- To provide insights of ASIC Design flow.
- To make the students aware of the current research and development in the VLSI industry.

Discussion Points of the Webinar

- Innovation in Electronic System Level design (ESL Design) and role of semiconductor/VLSI industry to boost it.
- Future trends in technology in VLSI industry like FinFET, Carbon nano tube etc.
- Prevailing and futuristic career opportunities, innovations /research in electronics industry.
- insights of ASIC Design flow

A Statement by the Expert

- "Attitude of continuous learning and enhancement in an engineer is the requirement of industry today." – Mr. Nilesh Ranpura

Glimpses of the Webinar